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10/531,949	04/19/2005	Masaru Minami	SON-2851	4516

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RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
GUHARAY, KARABI	
ART UNIT	PAPER NUMBER
2889	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,949	MINAMI, MASARU	
	Examiner	Art Unit	
	Karabi Guharay	2889	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment, filed on 8/25/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Amendment, filed on 8/25/2008 has been considered and entered.

Claims 1, 11 and 29 are amended.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 5, 11-12, 15-18, 21-22, 29-30, 33-36 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. (US 5811927), and further in view of Ando et al. (US 6,884,138).

Regarding claims 1 & 5, Anderson et al. disclose a flat -type display (cold cathode field emission display; Figs 9-10) comprising a first panel or anode plate (122 of Fig 3; liners 36-37 of column 5) and a second panel (cathode panel 164 of Fig 8), in which plurality of field emission devices (166) are formed and which are bonded to each other in their circumferential portions and having a space between the first panel and second panel, space being in vacuum state, in which a spacer (102) disposed between a first

panel effective field and a second panel effective field that work as display portion (lines 4-17 of column 8), said spacer is fixed to the first panel effective field and /or second panel effective field with a low-melting point metal material (bonding materials 168, 169 of Fig 9, are made of low melting point material such as gold or gold-palladium alloy; lines 1 and 47-49 of column 4), wherein a top surface of the spacer is electrically connected to the first panel (130 of Fig 9) through a conductive material layer (108) and a low melting point metal material (112), the conductive material layer (108) being between the top surface of the spacer and a low melting point metal material (112), wherein another top surface (109) of the spacer is electrically connected to an electrically conductive layer formed on the second panel (164) through a low melting point metal layer (169).

But Anderson does not disclose a conductive material being disposed between the other top surface (109) of the spacer and the low-melting point metal material layer (169).

However, in the same field of flat panel display, Ando et al. teaches the method of affixing spacers between first panel effective filed and second panel effective field (Fig 8) wherein both the top ends of the spacer (1020) is coated with a conductive material layer (206) and then a bonding material is attaching the coated top surface to the panels.

Ando et al. further teaches that providing such conductivity at the top surfaces of the insulating spacer results in clear color image having good color reproducibility since any distortion of the electric field is not generated (lines 52 of column 15- line 6 of column 16).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use conductive material layer at both the top surface of the spacer so as to prevent electric field distortion which in turn produce clear color image having the good color reproducibility.

Regarding claims 2, Anderson discloses that the spacer is formed of ceramic or glass (lines 35-37 of column 3).

Regarding claims 11, 15-16, 21-22, 29, 33-34 & 39-40, Anderson discloses a method for manufacturing a flat-type display, said flat-type display comprising a first panel or anode plate (122 of Fig 3; liners 36-37 of column 5) in which anode electrode and a phosphor layer are formed (lines 25-42 of column 6) and a second panel (cathode panel 164 of Fig 8) in which plurality of field emission devices (166) are formed, and which are bonded to each other in their circumferential portions and having a space between the first panel and the second panel, the space being in a vacuum state, a spacer (102) being disposed between a first panel effective field and a second panel effective field that work as display portion (lines 4-17 of column 8), the method comprising arranging a spacer (102) with a conductive material layer (108) formed on the top surface thereof and a low-melting-point (112 is made of low melting point material such as gold or gold palladium alloy lines 1 and 47-49 of column 4) metal material layer formed on one top surface of the conductive material layer, on the first panel effective field (130), then heating the low-melting-point metal material layer to melt the same and thereby fixing said spacer to the first panel effective field, the top surface of the spacer being electrically connected to the first panel through the conductive material layer and the low melting point metal material layer, and then placing the second panel on the other top surface of the spacer,

bonding the first panel and the second panel to each other in their circumferential portions, and vacuuming the space sandwiched between the first panel and the second panel (see claims 15 & 16).

But Anderson does not disclose another conductive material being disposed between the other top surface (109) of the spacer and the low-melting point metal material layer.

However, in the same field of flat panel display, Ando et al. teaches the method of affixing spacers between first panel effective filed and second panel effective field (Fig 8) wherein both the top ends of the spacer (1020) is coated with a conductive material layer (206) and then a bonding material is attaching the coated top surface to the panels.

Ando et al. further teaches that providing such conductivity at the top surfaces of the insulating spacer results in clear color image having good color reproducibility since any distortion of the electric field is not generated (lines 52 of column 15- line 6 of column 16).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use conductive material layer at both the top surface of the spacer so as to prevent electric field distortion which in turn produce clear color image having the good color reproducibility.

Regarding claims 12, 18, 30 & 36, Anderson discloses that the spacer is formed of ceramic or glass (lines 35-37 of column 3).

Regarding claims 17 & 35, combined method of Anderson & Ando discloses the method for manufacturing a flat-type display according to claim 29, in which a second low-melting-point metal material layer is formed on a portion where the spacer is to be

fixed in the second panel effective field, and, the second low-melting-point metal material layer is melted when the first panel and the second panel are bonded in their circumferential portions in said step (C), and thereby the spacer is fixed to the second panel effective field (see Fig 9 where both sides of the spacer are connected to each panel through low melting metal materials).

Regarding claims 4, 20 & 32 Anderson & Ando et al. disclose the flat-type display according to claims 1, 11 & 29, where the first panel and the second panel are bonded to each other in their circumferential portions (see bonding layer162) but is silent about layer is bonded through a material being made of a low-melting-point metal material. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use same low melting point metallic bonding layers (132) in the peripheral portion of the anode plate (122) to bond first and second panel through the side wall 162, since this facilitates manufacturing process as well as provide uniform height.

Claims 3, 13, 19, 31 & 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. & Ando et al. as applied to claims 1, 11 & 29 above, and further in view of Inoue et al. (2002/0079802).

Regarding claims 3, 13, 19, 31 & 37, Anderson discloses the flat panel display of claims 1, 11 & 29, where the first panel and the second panel are bonded to each other in their circumferential portions through a bonding layer (162) but is silent about layer being made of frit glass.

However, in the same field of endeavor, Inoue et al. that bonding the first and second panel in their circumferential portions through a bonding layer made of frit glass is old and conventional to form a vacuum enclosure (see paragraph 162).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate frit glass for bonding the first and second panel in the circumferential portion, since such bonding materials are well known suitable material for bonding two panel to form a vacuum enclosure for field emission device, and further, selection of known material for known purpose in within the skill of art.

Claims 6-7, 9-10, 23-24, 26-28, 41-42, 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al.& Ando et al. as applied to claims 1, 11 & 29 above, and further in view of Hsiao et al. (2002/0096992).

Regarding claims 6, 10, 23, 27-28, 41 & 45-46, Anderson et al. teach all the limitations of claim 6, 9, 23, 27-28, 41, 45-46, (see rejection of claims 1, 11 & 29) except for a plurality of spacer holders for temporarily holding the spacer in the first panel.

However, Hsiao et al. in the same field of Field emission device, teaches forming spacer holder (16 of Fig 5D) on the first panel (anode panel 1) where the spacers are hold temporarily before anodic bonding (paragraphs 21 & 34). Hsiao et al. further teach that such holder supports the spacer in the upper plate so as not to drop off before anodic bonding, further reduces the thickness of FED and does not increase any extra process before fixing the spacer by anodic bonding (see paragraphs 18-21).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate holder in the device of Anderson, as taught

by Hsiao et al. since such holder will reduce extra process for manufacturing FED and reduces the thickness of FED.

Regarding claims 7, 24, 42, Anderson discloses that the spacer is formed of ceramic or glass (lines 35-37 of column 3).

Regarding claims 9, 26, & 44, Anderson , Ando & Hsiao et al. discloses the flat panel display of claims 6, 23 & 41, together with the first panel and the second panels are bonded to each other in their circumferential portions (see bonding layer162) but is silent about layer is bonded through a material being made of a low-melting-point metal material. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use same low melting point metallic bonding layers (132) in the peripheral portion of the anode plate (122) to bond first and second panel through the side wall 162, since this facilitates manufacturing process as well as provide uniform height.

Claims 8, 25 & 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. & Ando et al. in view of Hsiao et al. (2002/0096992) and further in view of Inoue et al. (2002/0079802).

Regarding claims 8, 25, 43, Anderson & Hsiao et al. discloses the flat panel display of claims 6, 23 & 41, together with the first panel and the second panels are bonded to each other in their circumferential portions through a bonding layer (162) but are silent about layer being made of frit glass.

However, in the same field of endeavor, Inoue et al. teach that bonding the first and second panel in their circumferential portions through a bonding layer made of frit glass is old and conventional to form a vacuum enclosure (see paragraph 162).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate frit glass for bonding the first and second panel in the circumferential portion, since such bonding materials are well known suitable material for bonding two panel to form a vacuum enclosure for field emission device, and further, selection of known material for known purpose in within the skill of art.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al. & Ando et al. as applied to claim 1 above, further in view of Toyota et al. (US2003/0190772).

Regarding claim 47, Anderson & Ando et al. discloses all the limitations of claim 47, except for a partition wall formed on the substrate of the first panel between phosphor layers and a light absorbing layer formed between the substrate and the partition wall.

However, Toyota et al. in the same field of flat panel display, discloses partition wall formed on the substrate (30 of Fig 1)of the first panel (AP)between phosphor layers and a light absorbing layer formed between the substrate and the partition wall (see paragraphs 248-250). Toyota et al. further teaches that such partition between one phosphor to another phosphor on the anode substrate prevents optical cross talk and light absorbing layer between phosphor and between partition and the substrate provides improvement in the contrast of a display image.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate partition between different color phosphor in order to avoid color mixing and providing a light absorbing layer between the substrate and the partition so as to increase the contrast of the display.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is 571-272-2452. The examiner can normally be reached on Monday-Friday 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minh-Toan Ton can be reached on 571-272-2303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Karabi Guharay/
Primary Examiner, Art Unit 2889